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A New 1200V PT-IGBT with Protection Circuit employing the Lateral IGBT and Floating p-well Voltage Sensing Scheme

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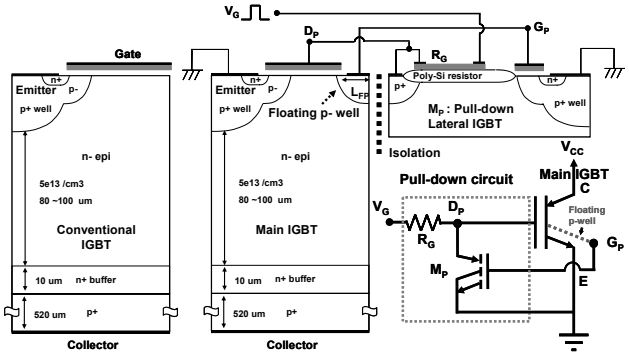
1. Introduction

It is well known that Insulated Gate Bipolar Transistor (IGBT) requires the short-circuit protections which protect the IGBT from the thermal destruction caused by the high power dissipation during the short-circuit condition.[1][2] Various fault protection circuits of IGBT such as current sensing scheme, de-saturation detection and V_{GE} detection have been reported. [2] The fault protection circuit usually focuses the short-circuit protection while the improvement of avalanche capability has not been considered. [3] However, the IGBT may experience the temporary avalanche breakdown during the inductive load switching due to the failure of free wheeling diode so that the avalanche energy should be considered together.[4] In order to increase the avalanche energy of IGBT besides the protection of the IGBT from short-circuit, we have already proposed the 600V PT-IGBT with protection circuit employing the lateral pull-down MOSFET and floating p-well voltage detection. [3][4] The chip area of lateral pull-down MOSFET should be increased to supply the enough current to the pull-down resistor in order to decrease the gate voltage of IGBT during the fault condition, so that the total area of protection circuit is increased to ensure the stable pull-down operation.

The purpose of this work is to propose a novel protection circuit of 1200V PT-IGBT employing the pull-down lateral IGBT (LIGBT) instead of lateral MOSFET in order to minimize the total area of protection circuit because the current handing capability of lateral IGBT (LIGBT) is better than that of lateral MOSFET due to the bipolar operation of IGBT.[5] We have also verified the floating p-well voltage saturation of the 1200V PT-IGBT according to cell pitch in order to protect the gate oxide of the pull-down transistor. 1200V PT-IGBT employing the protection circuit is fabricated using the planar IGBT process without any other additional mask. The forward I-V and blocking characteristics, switching and short-circuit behaviors are successfully measured.

2. Fault Sensing Scheme

Fig. 1 shows the cross-sectional view of fabricated devices. The pull-down lateral IGBT (M_P) and poly-Si resistor (R_G) are fabricated with the main IGBT using the same process.[3] M_P is isolated from the main IGBT. Fig. 2 (a) shows a unit-cell of the proposed IGBT employing the floating p-well. The floating p-well region is an opened emitter of vertical pnp structure such as p+ collector /n-drift/ floating p-well. The floating p-well voltage is saturated when the IGBT enters the high voltage current saturation mode because the depletion between the floating p-well and n-drift region moves the hole current flow from the p-base below the gate oxide to the bottom of p+ well because the voltage saturation of floating p-well decreases as the gate length (L_G) decreases. The floating p-well length (L_{FP}) has less dependency to floating p-well voltage because the vertical electric field of the junction between the floating p-well and n-drift region is independent to the L_{FP}. Threshold voltage (V_{TH}) of main IGBT and M_P are 4.1 V and 3.3 V, respectively. The width of M_P and resistance of R_G are 200 um and 500 ohms, respectively. The detection of faults is achieved by applying the voltage of floating p-well voltage to the gate of M_P.[3]



(a) conventional (b) proposed

Fig. 1 The cross-sectional view of the conventional IGBT(a) and the IGBT with the protection circuit using the proposed floating p-well voltage detection scheme(b) and the equivalent circuit

3. Experimental Results

As shown in Fig. 2 (b), the floating p-well voltage of main IGBT (voltage of G_P) without pull-down circuit is saturated while the collector voltage (V_{CE}) increases. The saturation voltage of G_P decreases as the gate length (L_G) is decreased due to the decrease of minority carriers in the adjacent floating p-well because the voltage of G_P is

proportional to the minority carrier density in the adjacent floating p-well. The current path of injected minority carriers from p+ collector is moved from the adjacent floating p-well under the gate oxide to the bottom of p+ well as the distance between the floating p-well and p+ emitter becomes shortened.[4] Fig. 2 (c) shows that the voltage of G_P does not increase above V_{TH} of M_P under the forward blocking state which avoids the false detection of faults and gate oxide failure of M_P. The voltage of G_P also decreases under the forward blocking state as the L_G is decreased due to the improved curvature of depletion boundary.[4] The forward voltage drop of the proposed IGBT at the 100 A/cm^2 is rather increases by 0.1V compared to that of conventional IGBT due to the JFET resistance.[4] Fig. 3 shows that I_C is decreased by the turn-on of M_P when the voltage of G_P increases above the V_{TH} of M_P.

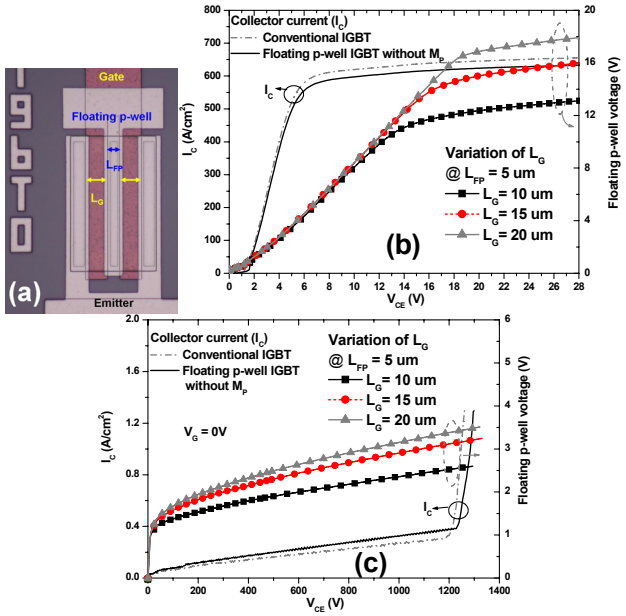


Fig. 2 Top-view of the unit-cell of 1200V PT-IGBT (a), measured forward I-V (b) and blocking characteristics (c) of main IGBT without M_P according to various gate length (L_G)

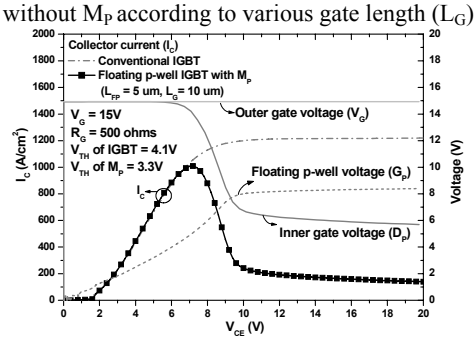


Fig. 3 Measured forward I-V of main IGBT employing the pull-down LIGBT

Fig. 4 shows the short-circuit behaviors under the hard switching fault (HSF) and fault under load (FUL) condition. The collector of main IGBT is subjected to V_{CC} of 600V under the both conditions. The voltage of D_P is successfully decreased under the fault conditions due to the turn-on of M_P by detecting the voltage of G_P. In order to investigate the effect of pull-down circuit on the switching behaviors, inductive load switching characteristics were measured. The M_P is not turned on during the normal turn-on transients because the voltage of G_P does not increase above the V_{TH} of M_P.

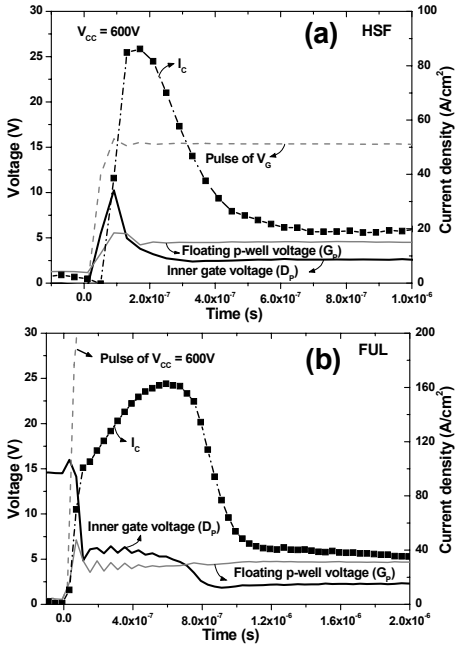


Fig. 4 Measured short-circuit behaviors under HSF(a) and FUL(b)

4. Conclusion

We have successfully fabricated and verified a new protection circuit employing the pull-down LIGBT and floating p-well voltage sensing scheme. The experimental results show that the proposed protection circuit successfully protects the 1200V PT-IGBT by sensing the fault signal of floating p-well during both hard switching fault (HSF) and fault under load (FUL) conditions with reducing the total chip area of protection circuit. The width of the pull-down transistor is considerably reduced from 2000 um to 200 um by replacing the lateral MOSFET with the lateral IGBT. The floating p-well voltage saturation decreases as the gate length is reduced. The optimum cell pitch of the IGBT protects the gate oxide breakdown of protection circuit without the clamp of the pull-down transistor.

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