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(54) METHOD FOR FABRICATING AT LEAST ONE TRANSISTOR

(75) Inventors: **Shu Yuan**, Singapore (SG); **Xuejun Kang**, Singapore (SG); **Shi Ming Lin**, Singapore (SG)

(73) Assignee: **Tinggi Technologies Private Limted**, Singapore (SG)

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H01L 21/50 (2006.01)
(52) **U.S. Cl.** **438/122**; 438/121; 438/E21.403
(58) **Field of Classification Search** 438/122–125, 438/705–720; 257/192–195, 712–706, 77–79, 257/98–103
See application file for complete search history.

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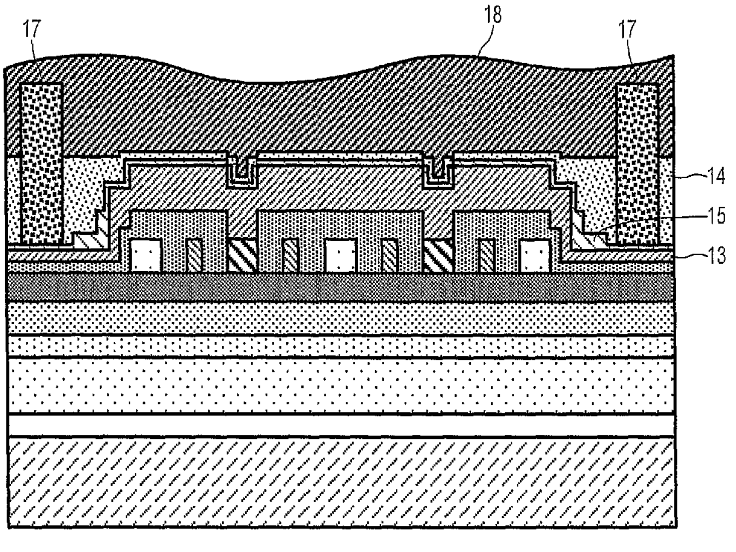
Primary Examiner — Dung A Le
(74) *Attorney, Agent, or Firm* — Blakely, Sokoloff, Taylor & Zafman LLP.

(57) **ABSTRACT**

A method for fabricating transistors such as high electron mobility transistors, each transistor comprising a plurality of epitaxial layers on a common substrate, method comprising: (a) forming a plurality of source contacts on a first surface of the plurality of epitaxial layers; (b) forming at least one drain contact on the first surface; (c) forming at least one gate contact on the first surface; (d) forming at least one insulating layer over and between the gate contacts, source contacts and the drain contacts; (e) forming a conductive layer over at least a part of the at least one insulating layer for connecting the source contacts; and (f) forming at least one heat sink layer over the conductive layer.

9 Claims, 10 Drawing Sheets



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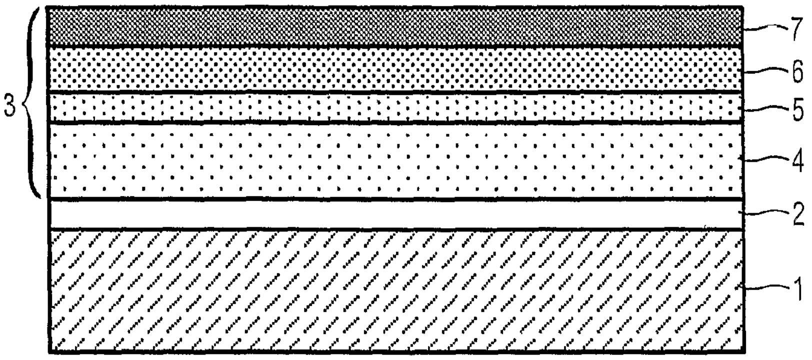

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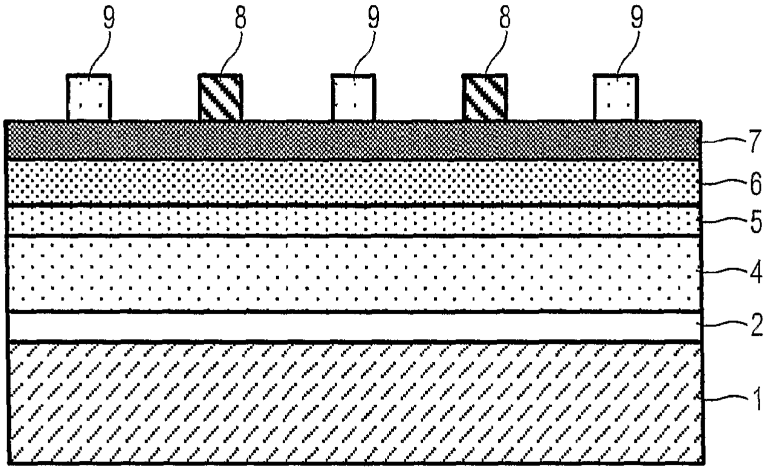

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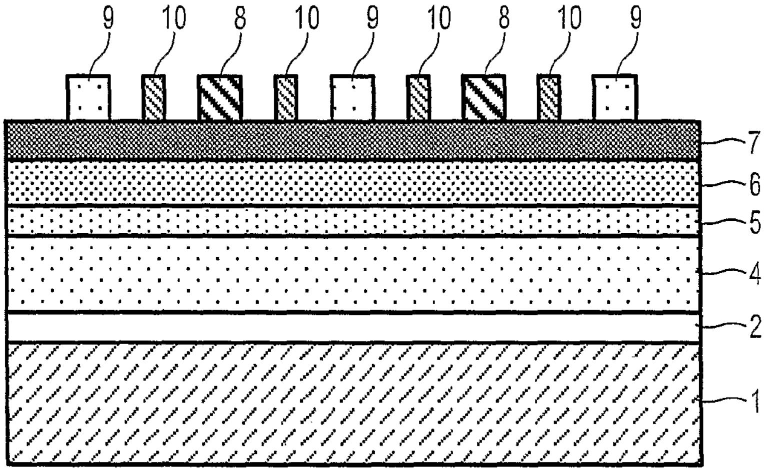

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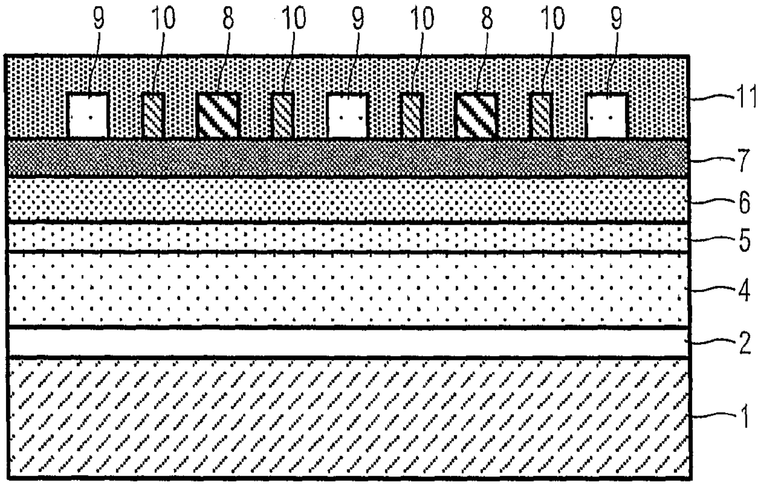

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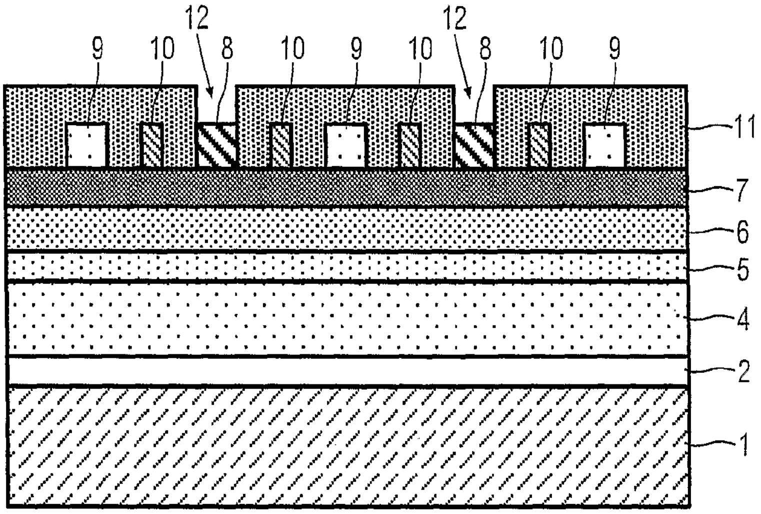

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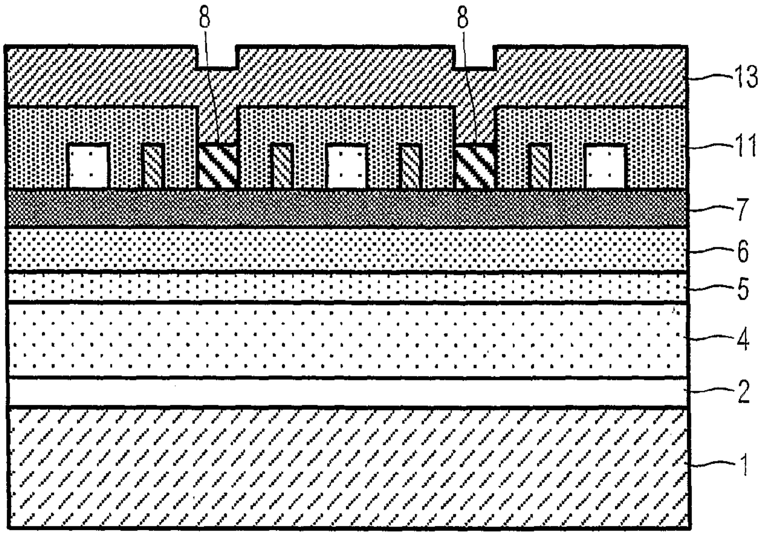

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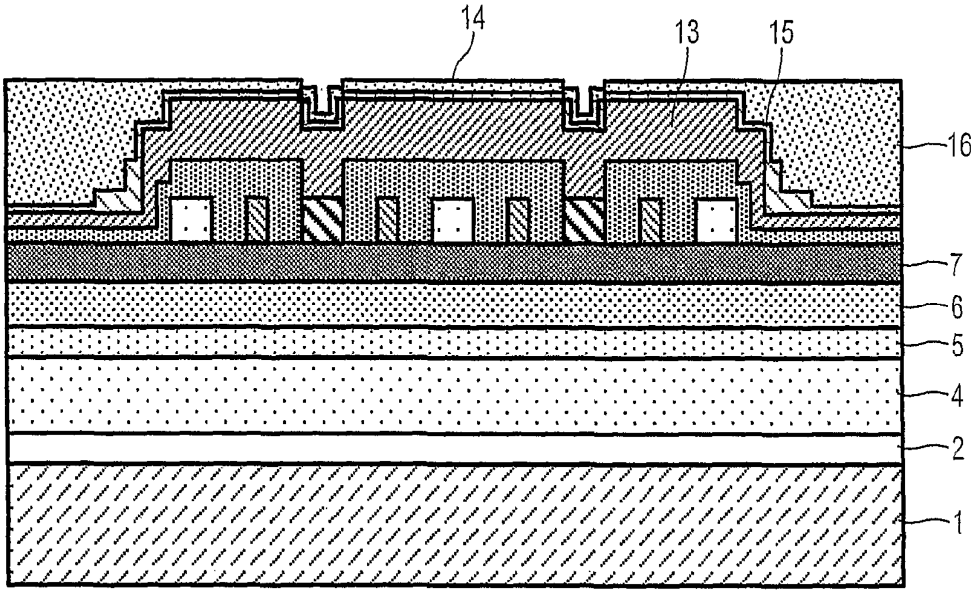

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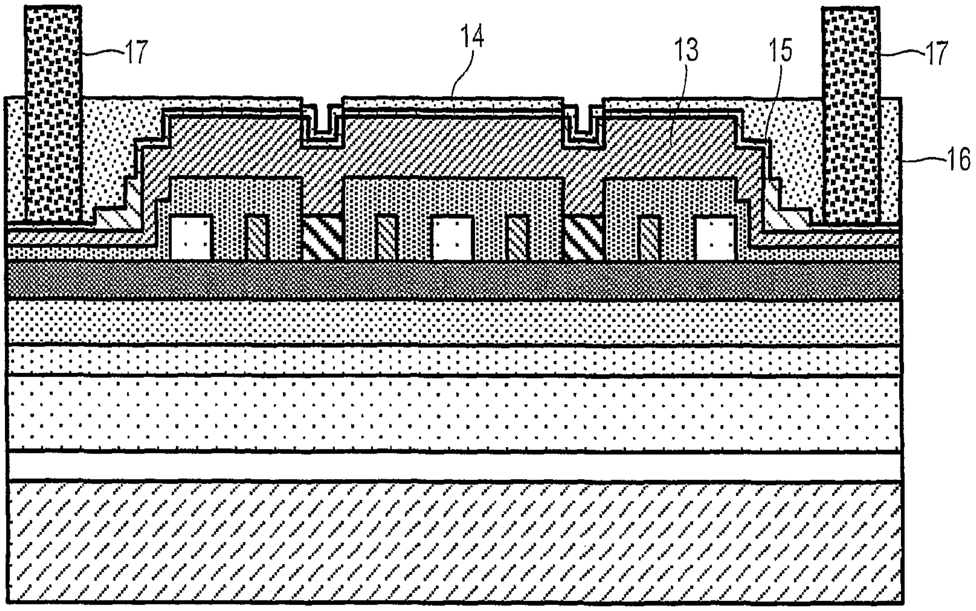

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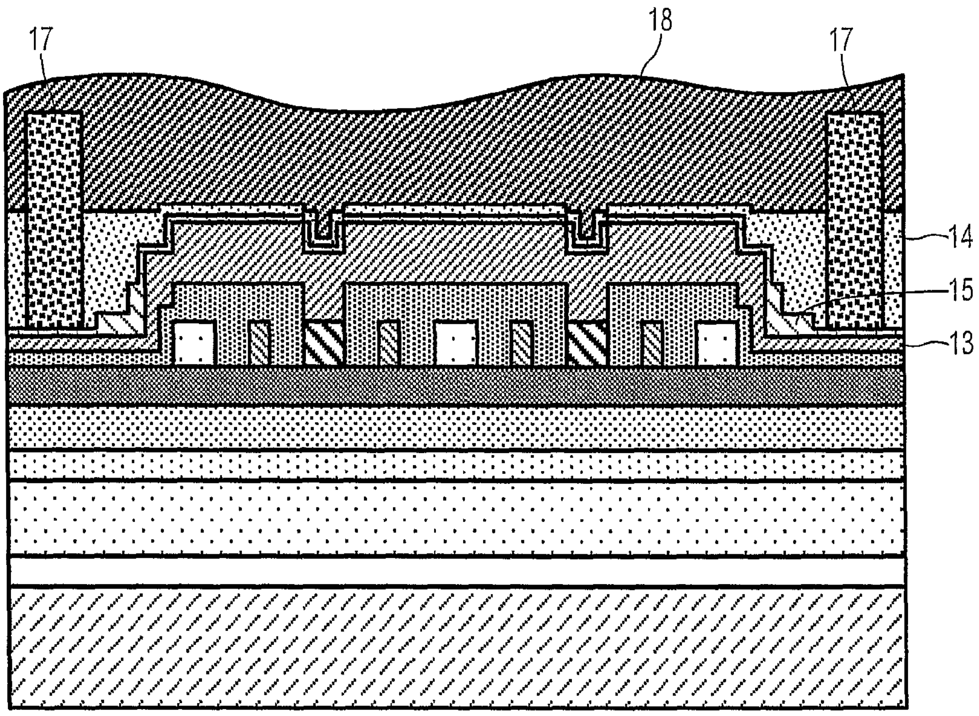

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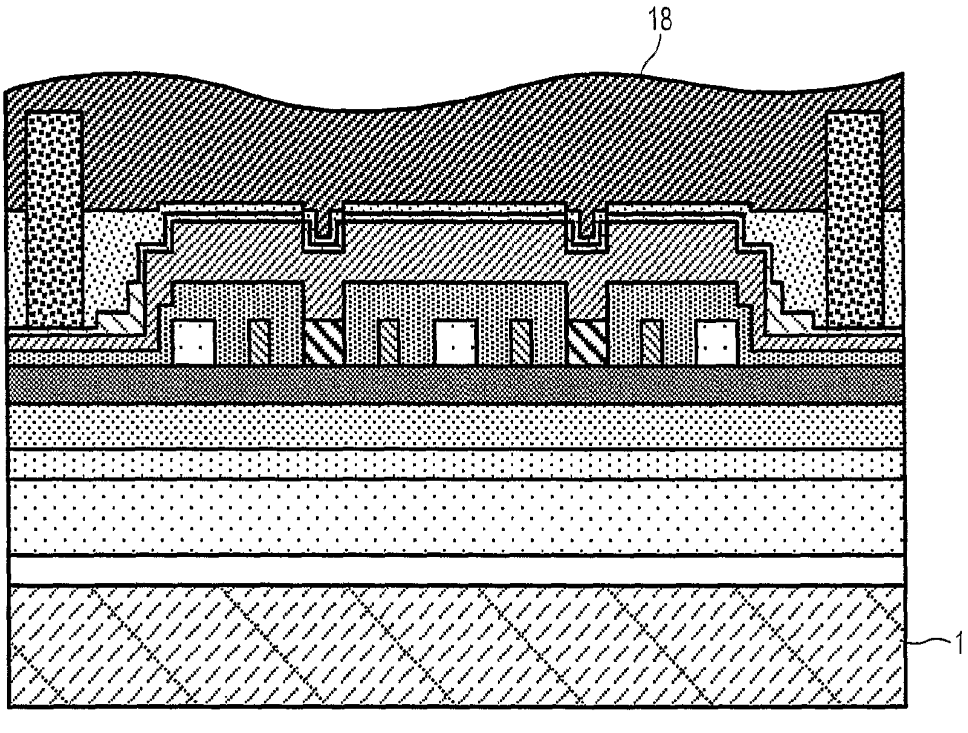

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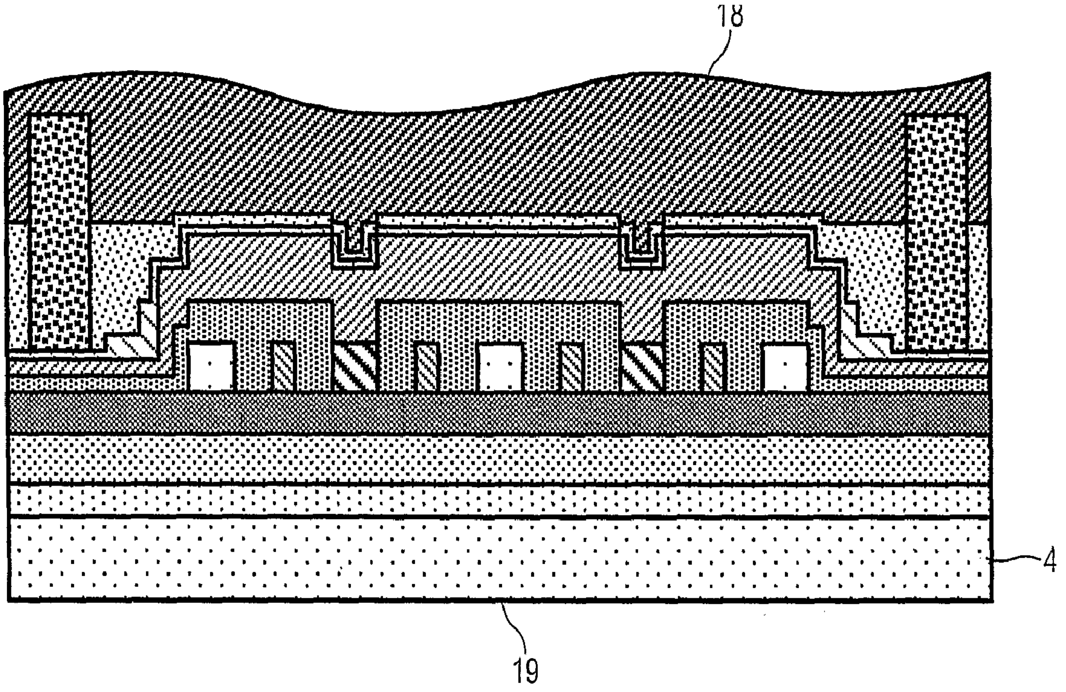

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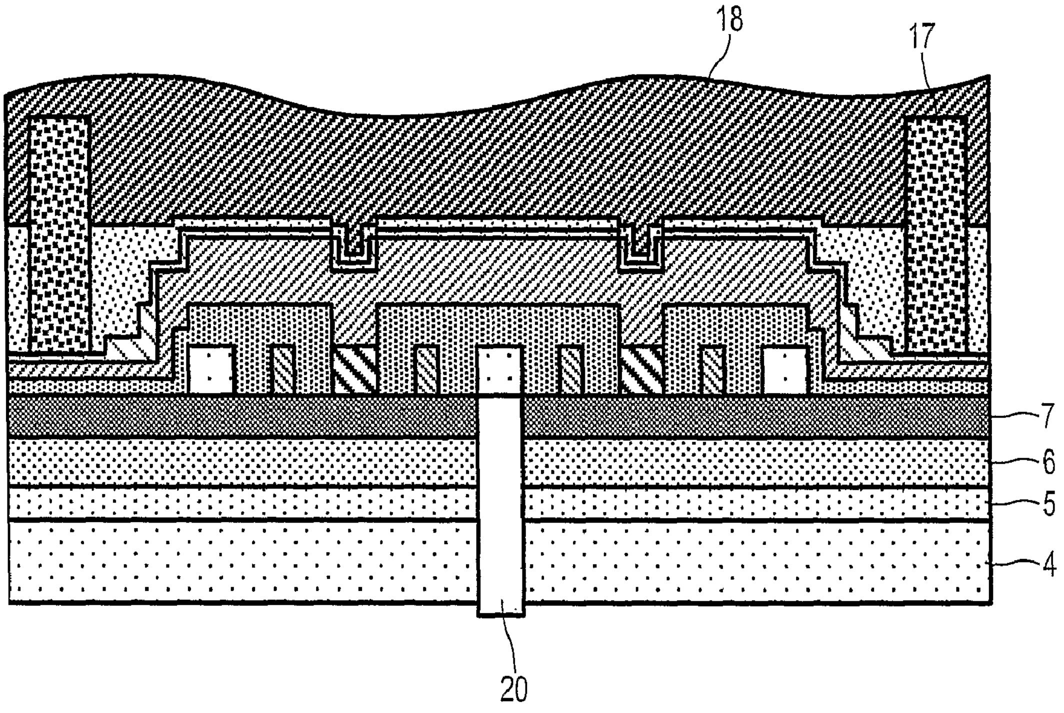

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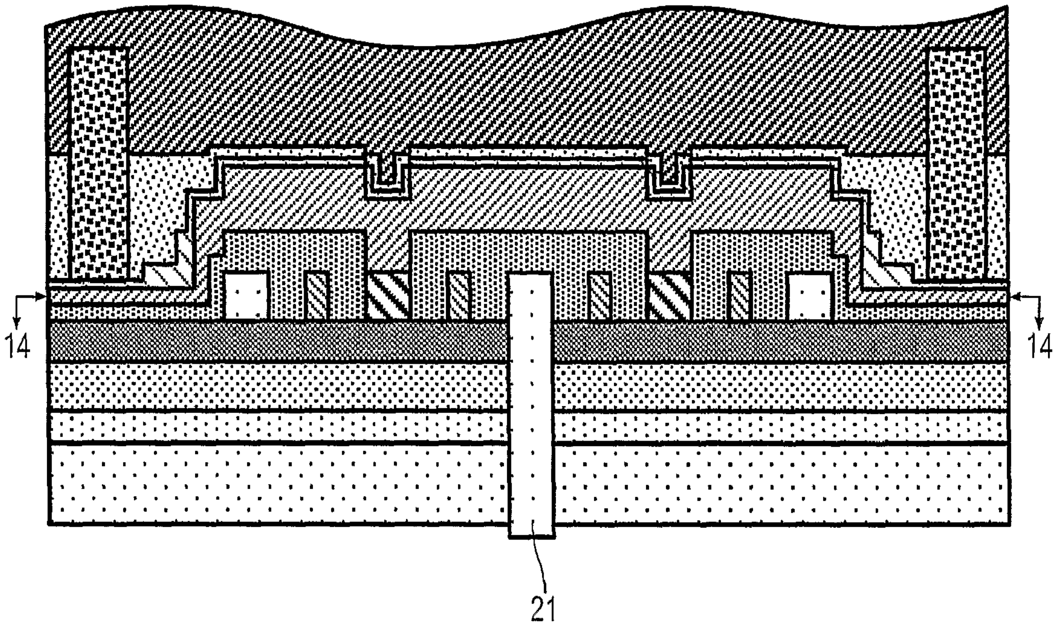

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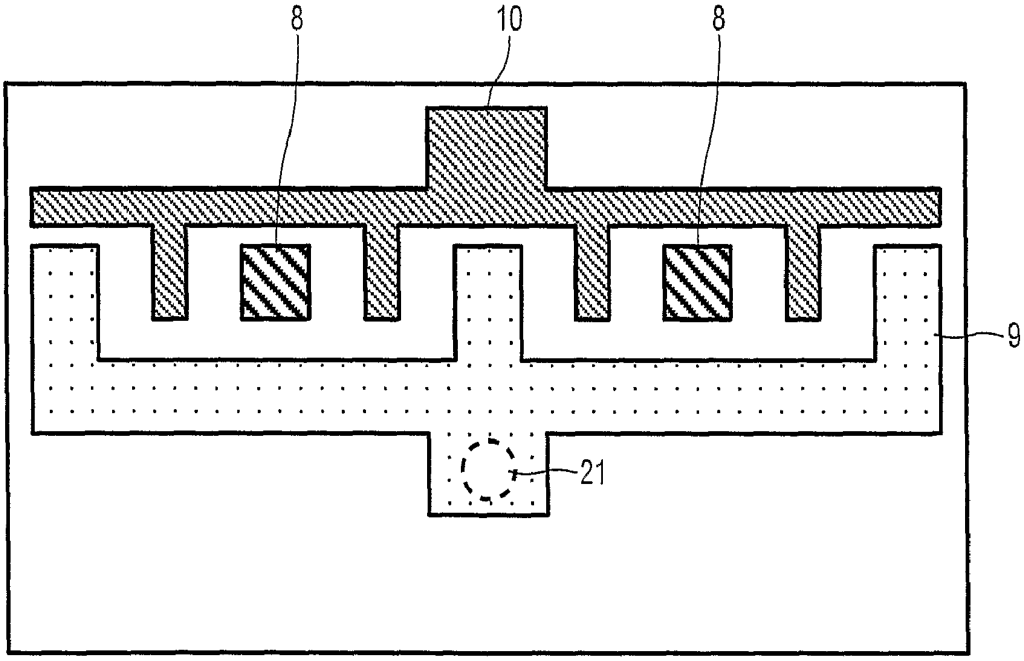

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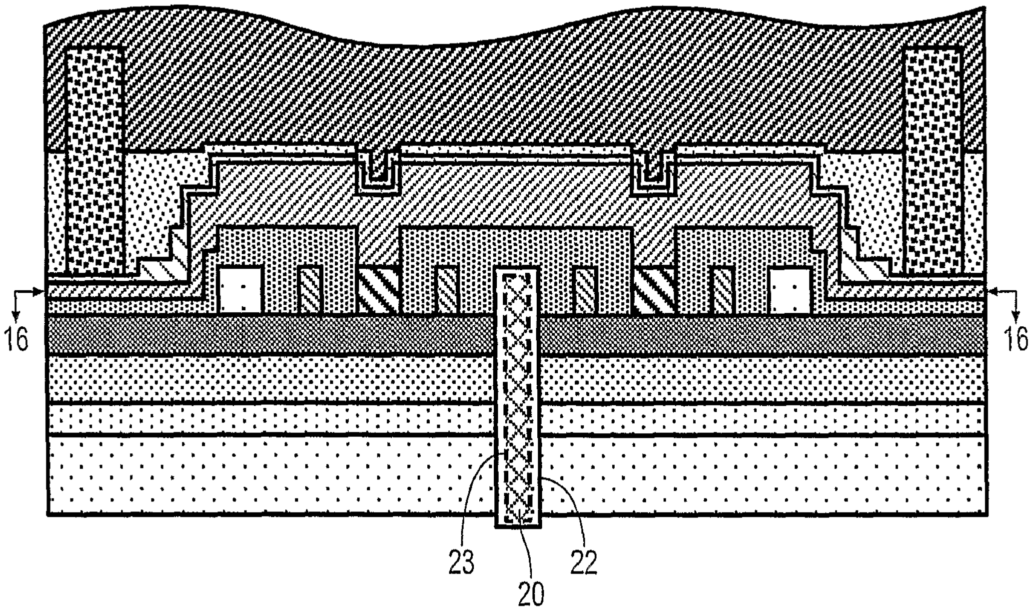


FIG. 15

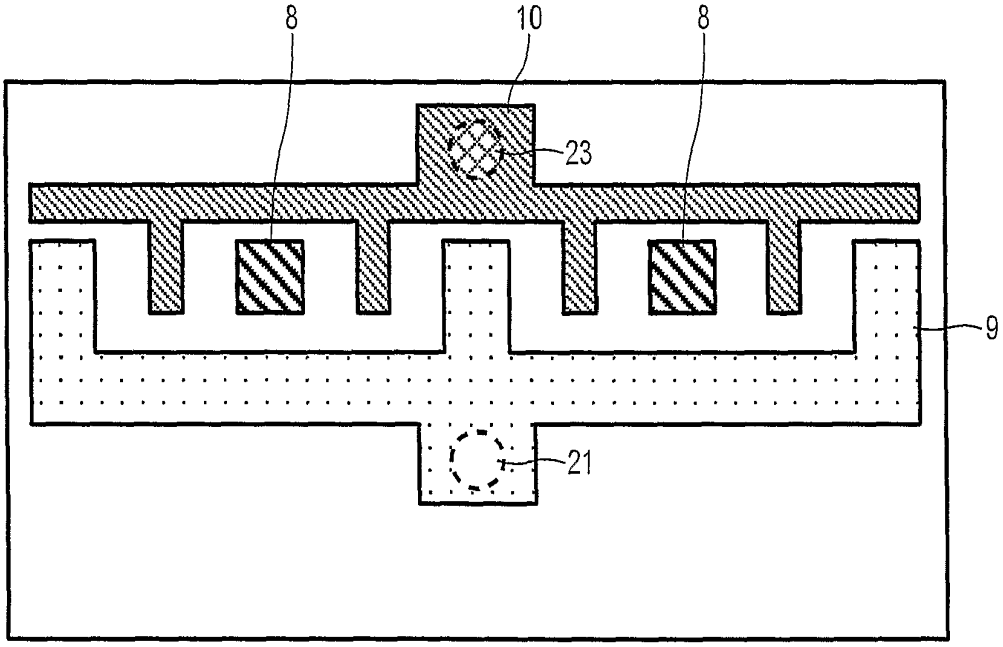


FIG. 16

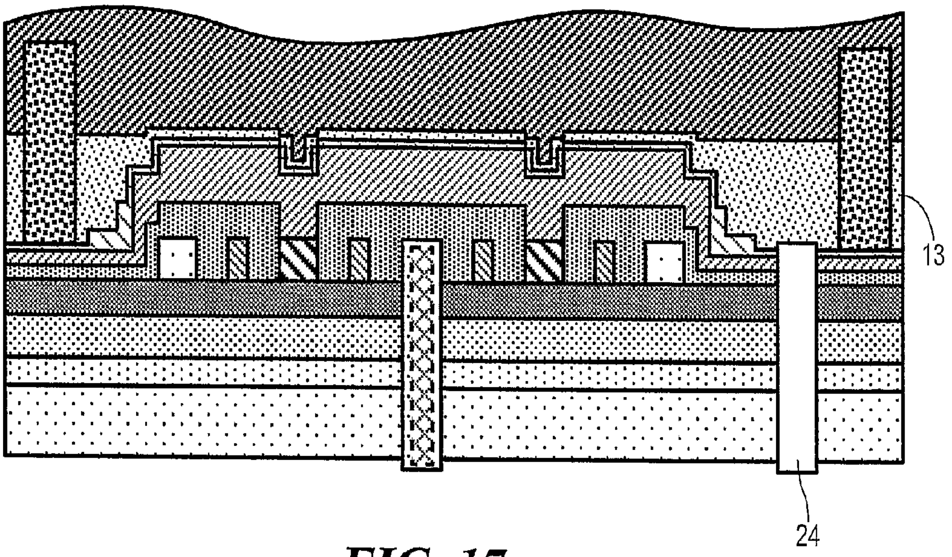
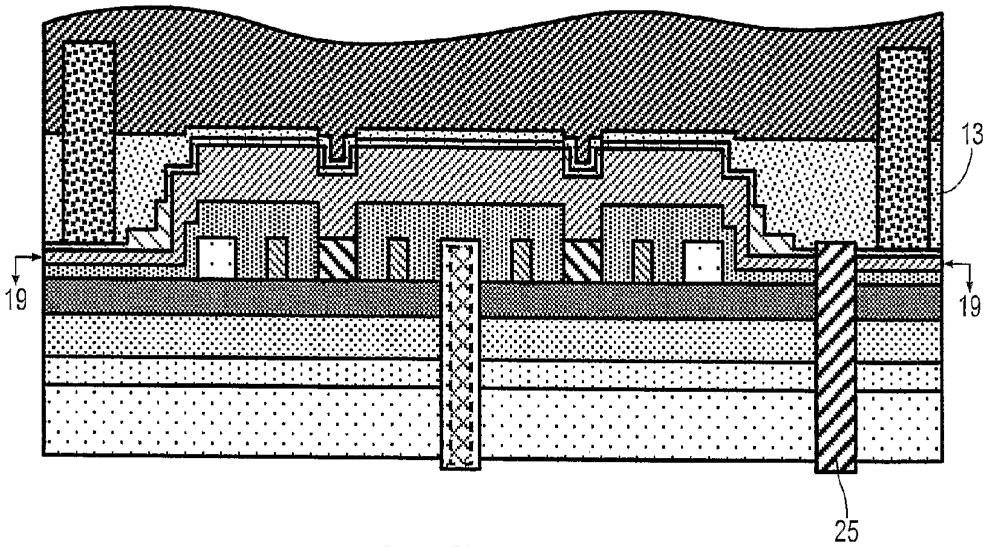


FIG. 17



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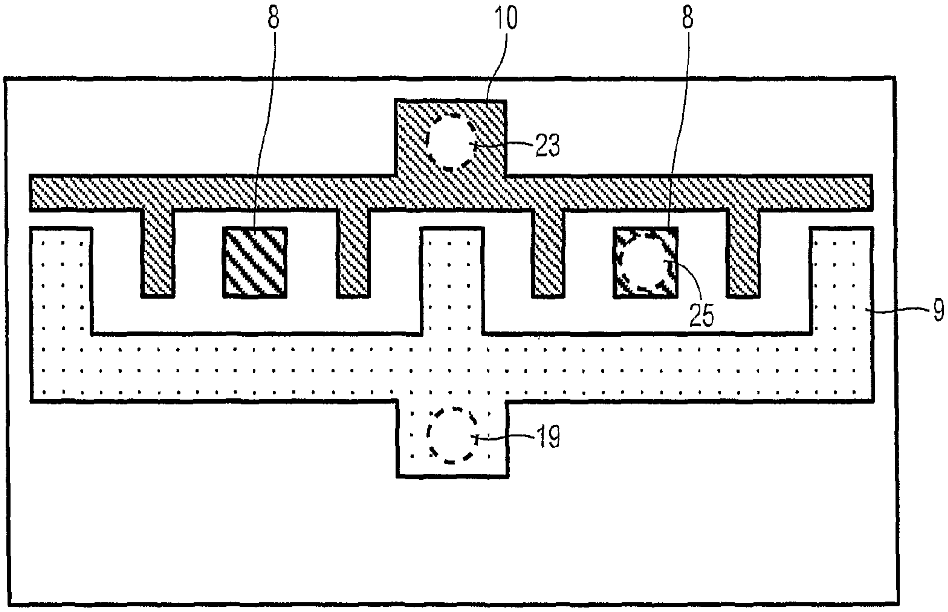

FIG. 19

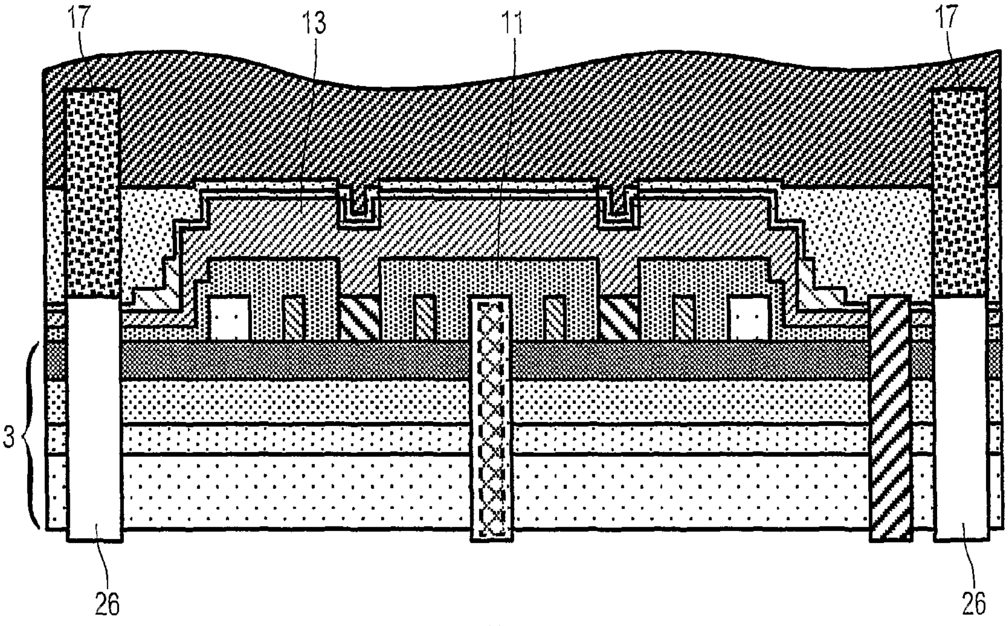

FIG. 20

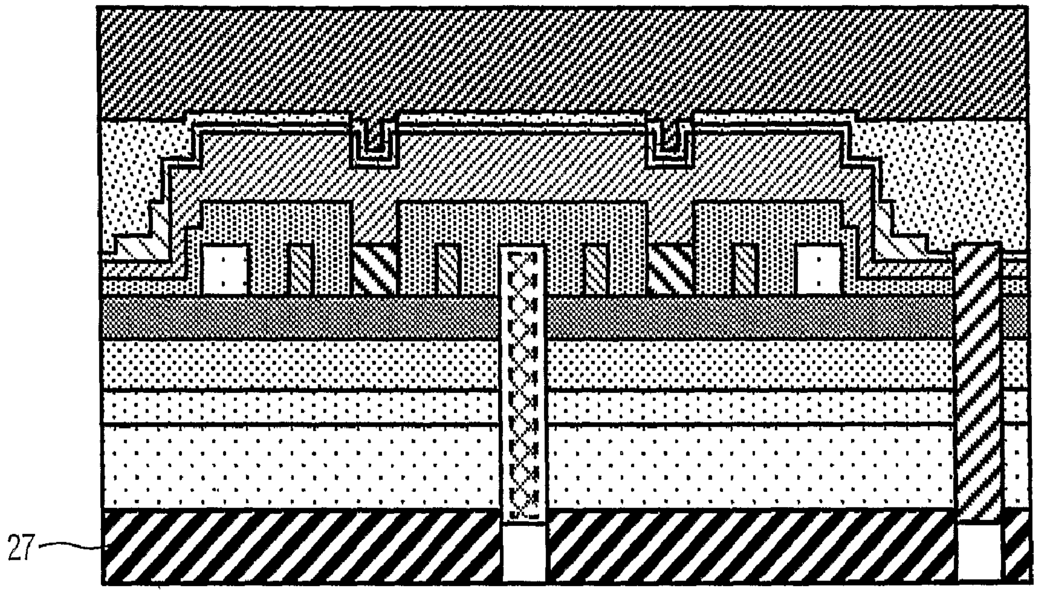

FIG. 21

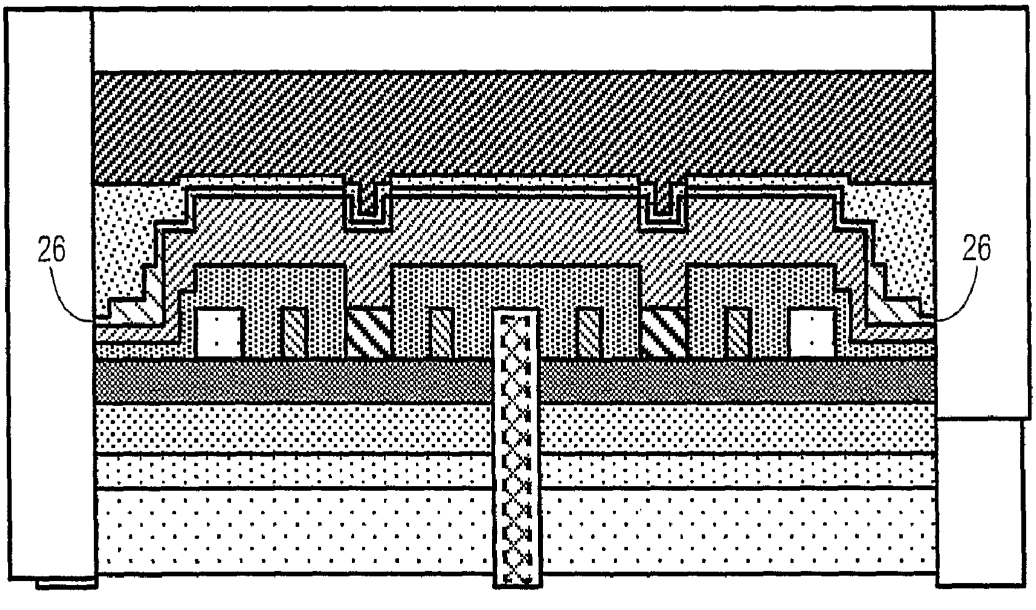

FIG. 22

METHOD FOR FABRICATING AT LEAST ONE TRANSISTOR

CROSS-REFERENCE TO OTHER APPLICATIONS

This is a National Phase of International Application No. PCT/SG2006/000255, filed on Sep. 1, 2006, which claims priority from Singaporean Patent Application No. 200506897-8, filed on Oct. 19, 2005.

FIELD OF THE INVENTION

This invention relates to the fabrication of transistors and refers particularly, though not exclusively, to the fabrication of gallium nitride high electron mobility transistors ("HEMT") and to transistors so fabricated.

BACKGROUND OF THE INVENTION

HEMT devices have been proposed for a few years. They are capable of high power with over 100 W/chip being possible; high frequency—1 to 40 GHz being possible; and can operate at temperatures of over 600° C. This generates a lot of heat so heat dissipation becomes important as not all devices can withstand such temperatures, and the HEMT device may be used with many other devices.

SUMMARY OF THE INVENTION

In accordance with a first preferred aspect there is provided a method for fabricating transistors, each transistor comprising a plurality of epitaxial layers on a substrate, method comprising:

- forming a plurality of source contacts on a first surface of the plurality of epitaxial layers;
    - forming at least one drain contact on the first surface;
    - forming at least one gate contact on the first surface;
    - forming at least one insulating layer over and between the gate contact, source contacts and drain contact to insulate the gate contact, source contacts and the drain contact;
    - forming a conductive layer-over and through at least a part of the at least one insulating layer for connecting the source contacts; and
    - forming at least one heat sink layer over the conductive layer.

According to a second preferred aspect there is provided an apparatus comprising transistors, each transistor comprising:

- a plurality of epitaxial layers having a first surface;
    - a plurality source contacts, at least one drain contact, and at least one gate contact, all on the first surface;
    - at least one insulating layer over and between the gate contact, source contacts and drain contact for insulating the gate contact, source contacts and the drain contact;
    - a conductive layer over and through at least a part of the at least one insulating layer for connecting the source contacts; and
    - at least one heat sink layer over the conductive layer.

The transistors may be high electron mobility transistors. The plurality of epitaxial layers may comprise a layer of gallium nitride, a layer of aluminium gallium nitride, a layer of n+ aluminium gallium nitride and a final layer of gallium nitride. The first surface may be on the final layer of gallium nitride. The conductive layer may connect the plurality of source contacts through vias in the at least one insulating layer. The at least one insulating layer may be heat conductive and electrically insulating.

A relatively thick layer of a heat conductive metal may be formed over the conductive layer. At least one seed layer may be formed on the conductive layer before the relatively thick layer is formed.

The drain, gate and source connections may be formed by creating then filling vias through the substrate and the epitaxial layers to the drain contact, gate contact and the conductive layer respectively.

Alternatively, the substrate may be removed and the drain, gate and source connections formed by creating then filling vias through the expitaxial layers to the drain contact, gate contact and conductive layer respectively. In this case, a further layer of heat conductive but electrically insulating material may be applied in place of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the present invention may be fully understood and readily put into practical effect, there shall now be described by way of non-limitative example only preferred embodiments of the present invention, the description being with reference to the accompanying illustrative drawings.

In the drawings:

FIG. **1** is a schematic illustration of a device at a first stage of the fabrication process;

FIG. **2** is a schematic illustration of the device at a second stage of the fabrication process;

FIG. **3** is a schematic illustration of the device at a third stage of the fabrication process;

FIG. **4** is a schematic illustration of the device at a fourth stage of the fabrication process;

FIG. **5** is a schematic illustration of the device at a fifth stage of the fabrication process;

FIG. **6** is a schematic illustration of the device at a sixth stage of the fabrication process;

FIG. **7** is a schematic illustration of the device at a seventh stage of the fabrication process;

FIG. **8** is a schematic illustration of the device at an eighth stage of the fabrication process;

FIG. **9** is a schematic illustration of the device at a ninth stage of the fabrication process;

FIG. **10** is a schematic illustration of the device at a tenth stage of the fabrication process;

FIG. **11** is a schematic illustration of the device at an eleventh stage of the fabrication process;

FIG. **12** is a schematic illustration of the device at a twelfth stage of the fabrication process;

FIG. **13** is a schematic illustration of the device at a thirteenth stage of the fabrication process;

FIG. **14** in a full cross-sectional view along the lines and in the direction of arrows **14-14** on FIG. **13**;

FIG. **15** is a schematic illustration of the device at a fourteenth stage of the fabrication process;

FIG. **16** a full cross-sectional view along the lines and in the direction of arrows **16-16** on FIG. **15**;

FIG. **17** is a schematic illustration of the device at a fifteenth stage of the fabrication process;

FIG. **18** is a schematic illustration of the device at a sixteenth stage of the fabrication process;

FIG. **19** is a full cross sectional view along the lines and in the direction of arrows **19-19** on FIG. **18**;

FIG. **20** is a schematic illustration of the device at a seventeenth stage of the fabrication process;

FIG. **21** is a schematic illustration of the device at a final stage of the fabrication process; and

FIG. **22** is a schematic illustration of the device at an alternative final stage of the fabrication process.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** shows the structure at the commencement of fabrication. A sapphire substrate **1** has a buffer layer **2** above it, and the epitaxial layers **3** are on the buffer layer **2**. The epitaxial layers **3** comprise a layer **4** of GaN, a layer **5** of AlGaN, and n+ layer **6** of AlGaN, and a final GaN layer **7**.

Source **8** and drain **9** contacts are then formed on the surface of the final GaN layer (FIG. **2**) there being a source **8** and a drain contact **9** for each transistor. Gate contacts **10** are then formed between each source contact **8** and each drain contact **9** (FIG. **3**). In this way when each gate **10** is activated current will flow from one source **8** to the two drains **9**, one on each side of source contact **8**.

As shown in FIG. **4**, an electrically insulating layer such as a passivation layer **11** of, for example AlN, is then applied to electrically insulate the contacts **8**, **9**, **10** while being able to conduct heat. The layer **11** is preferably heat conductive. A resist is applied over passivation layer **11** (FIG. **5**) and vias **12** formed through passivation layer **11** down to the source contacts **8** and the resist removed. A further layer **13** of an electrically and heat conductive metal is applied over the passivation layer **13**, the layer **16** also filling the vias **12**. This connects the source contacts **8** (FIG. **6**). In this way, all contacts **8**, **9** and **10** are in the one plane.

As shown in FIG. **7**, at least one further layer **14** is applied over the conductive metal layer **13** and the passivation layer **11** not covered by the conductive metal layer **13**. The further layer **14** is a seed layer.

The seed layer **14** may be a number of layers—for example, three different metal layers. The first seed layer should adhere well to the conductive layer **13** and may be of chromium or titanium. It may be followed by second layer and third layer that may be of tantalum and copper respectively. Other materials may be used for all seed layers. The second seed layer may act as a diffusion barrier, preventing copper or other materials placed on top of it (such as, for example, the third seed layer) from diffusing, into the expitaxial layers **3**. The third seed layer acts as a seeding layer for subsequent electroplating.

As shown, there are two layers **15**, **16** with the layer **15** acting as the diffusion barrier and the other layer **16** being the seeding layer.

The coefficients of thermal expansion of the seed layers may be different from that of GaN which is 3.17. While the thermal expansion coefficients of the contact layers **13** may be different from that of GaN (they are 14.2 and 13.4 respectively), they are relatively thin (a few nanometers) and do not pose serious stress problems to the underlining GaN epitaxial layers. However, plated copper to be added later may be as thick as hundreds of microns and thus may cause severe stress problems. Thus, the seed layers can be used to buffer the stress. This may be by one or more of:

by having sufficient flexibility to absorb the stress,

by having sufficient internal slip characteristics to absorb the stress,

by having sufficient rigidity to withstand the stress, and

by having graded thermal expansion coefficients.

In the case of graded thermal coefficients, that of the first layer preferably less than that of the second layer and that of the second layer is preferably less than that of the third layer and so forth. For example, as shown the first layer **15** may be tantalum with a coefficient of thermal expansion of 6.3, and the second layer **6** may be copper with a coefficient of thermal expansion of 16.5. In this way the coefficients of thermal expansion are graded from the passivation layer **13** and to the outer, copper layer **18**. An alternative is to have coefficients of expansion that differ such that at the temperatures concerned, one metal layer expands while another contracts.

If the outer, copper layer **18** was applied directly to the contact layer **13** and passivation layer **11**, the differences in their thermal expansion rates may cause cracking, separation, and/or failure. By depositing a plurality of seed layers of different materials, particularly metals each having a different coefficient of thermal expansion, the stresses of thermal expansion are spread through the seed layers with the resultant lower likelihood of cracking, separation and/or failure. If there are intermediate layer(s), the intermediate layer(s) should have coefficient(s) of expansion between those of layers **15** and **16**, and should be graded from that of the first layer **15** to that of the final layer **16**. There may be no intermediate layer, or there may be any required or desired number of intermediate layers (one, two, three and so forth).

For patterned plating of a layer **18** of relatively thick metal such as copper that will serve as the new substrate and/or heat sink, a pattern of thick resists **17** is applied to the seed layer **15** by standard photolithography (FIG. **8**), and the remaining metal **18** is plated between and over the thick resists **17** (FIG. **9**) to form a single metal support layer **18**.

The removal or lift-off of the sapphire substrate **1** then takes place (FIGS. **10** and **11**) in accordance with known techniques such as, for example, that described in Kelly [M. K. Kelly, O. Ambacher, R. Dimitrov, R. Handschuh, and M. Stutzmann, phys. stat. sol. (a) 159, R3 (1997)]. The substrate **1** may also be removed by polishing or wet etching. This exposes the lowermost surface **19** of the GaN layer **4**. It is preferred for lift-off of the substrate to take place while the epitaxial layers **3** are intact to improve the quality of removal, and for structural strength. By having the epitaxial layers **3** intact at the time of removal the electrical and mechanical properties of the epitaxial layers **3** are preserved.

After the removal of the original substrate **1**, the thickly plated metal **18** is able to act as one or more of: the new mechanical support; and during operation of the semiconductor device is able to act as one or more of: a heat sink, a heat dissipater, and a connecting layer. As the final GaN layer **7** is relatively thin, the heat generated in active layers **3** is more easily able to be conducted to the thick layer **18**. Also, each of the layers **11**, **13** and **14** are heat conductive.

The seed layer(s) **14** may be an electrical insulating layer but must be a good thermal conductor e.g. AlN.

The thick layer **18** creates a parasitic capacitance that slows the speed of operation. By increasing the distance between layer **18** and the epitaxial layers **3**, the parasitic capacitance is decreased.

A resist layer is applied to the now-exposed surface **19** of the GaN layer **4** and etching takes place to form at least one via **20** through epitaxial layers **13** to the drain contact **9** (FIG. **12**). Via **20** is then filled (FIG. **13**) to form a drain connection **21**. FIG. **14** show a view of the drain connection **20**, source contacts **8** and gate contacts **10**.

A separate via **22** is formed (FIG. **15**) through the epitaxial layers **3** to the gate contact **10** and via **22** is filled to form a gate connection **23**.

FIG. **16** shows a view of the gate connection **23** as well as the drains connection **20**, and source contact **8**.

FIGS. **17** and **18** show a similar process for the source connection **8**. A via **24** is formed through the expitaxial layers **3** to the source connector layer **13** and the via **24** filled to form the source connection **25**.

FIG. **19** shows a view of the source connection **25**.

Etching then takes place (FIG. **20**) to form gaps **26** through the epitaxial layers **3**, passivation layer **11** and conductive layer **13** until the ends of the thick resists **17** are exposed. The thick resists **17** are then removed for die separation.

This leaves the connections **20**, **23** and **25** so the device can be electrically connected. Alternatively, and as shown in FIG. **22**, the process of FIGS. **17** and **18** may be avoided with die separation being as described above. Electrical connection for the source contact layer **13** will then be at either or both sides **26**.

If desired, the substrate **1** may be left in place and holes drilled by, for examples, lasers to enable the connections **20**, **23** and **25** to be formed. Alternatively, and as shown in FIG. **21**, a further layer **27** of a material that is a heat conductive but electronically insulating (e.g. AlN) may be added in place of substrate **1**.

In this way the device HEMT device can be used with the relatively thick metal layer **18** acting as one or more of: a contact, heat sink, heat diffuser, and a physical support for the device. The combined effect of the passivation layer **11**, the conductive layer **13**, the seed layer **14** and the relatively thick layer **18** is that they are all conductive so they all combine to conduct heat away from the epitaxial layers **3**, and for them to combine to be a heat sink.

Whilst there has been described in the foregoing description preferred embodiments of the present invention, it will be understood by those skilled in the technology concerned that many variations or modifications in details of design or construction may be made without departing from the present invention.

What is claimed is:

1. A method for fabricating transistors, each transistor comprising a plurality of epitaxial layers on a common substrate, the method comprising:

forming a plurality of source contacts on a first surface of the plurality of epitaxial layers;

forming at least one drain contact on the first surface;

forming at least one gate contact on the first surface;

forming at least one layer of insulating material over and between the at least one gate contact, the plurality of source contacts and the at least one drain contact for insulating the at least one gate contact, the plurality of source contacts and the at least one drain contact;

forming a conductive layer over and through at least a part of the at least one insulating layer, the conductive layer connecting the plurality of source contacts;

forming at least one seed layer on the conductive layer; and

forming at least one heat sink layer over the at least one seed layer; and

wherein the at least one seed layer is configured to buffer stresses of thermal expansion caused by the at least one heat sink layer.

2. The method as claimed in claim **1**, wherein the transistors are high electron mobility transistors, the plurality of epitaxial layers comprising a layer of gallium nitride, a layer of aluminum gallium nitride, a layer of n+ aluminum gallium nitride and a final layer of gallium nitride, the first surface being on the final layer of gallium nitride, the at least one layer of insulating material being electrically insulating but heat conductive, the conductive layer connecting the plurality of source contacts through vias in the at least one layer of insulating material.

3. The method as claimed in claim **1**, wherein the at least one heat sink layer is a relatively thick layer of conductive metal formed over the at least one seed layer, the relatively thick layer of conductive metal being for at least one selected from the group consisting of: a structural support, a heat sink, a heat dissipater, and as a connector.

4. The method as claimed in claim **1**, wherein the seed layer comprises a plurality of seed layers, wherein a first of the plurality of seed layers is applied to the conductive layer, the first of the plurality of seed layers being of a material that has a first co-efficient of thermal expansion, and a second seed layer is formed on the first of the plurality of seed layers, the second seed layer being of a material that has a second co-efficient of thermal expansion, the second co-efficient of thermal expansion being greater than the first co-efficient of thermal expansion, one of the first of the plurality of seed layers and the second seed layer being a diffusion barrier for providing a barrier to diffusion of a layer applied to it from diffusing into the epitaxial layers.

5. The method as claimed in claim **1**, wherein a source connection is formed by creating then filling at least one via through the common substrate and the plurality of epitaxial layers to the conductive layer.

6. The method as claimed in claim **1**, wherein a drain connection is formed by creating then filling at least one via through the common substrate and the plurality of epitaxial layers to the at least one drain contact, a gate connection is formed by creating then filling at least one via through the common substrate and the plurality of epitaxial layers to the at least one gate contact, and a source connection is formed by forming then filling at least one via through the plurality of epitaxial layers to the conductive layer.

7. The method as claimed in claim **1**, further comprising removing the common substrate after the at least one heat sink layer is formed, and forming a further layer of electrically insulating and heat conductive material in place of the common substrate.

8. The method as claimed in claim **7**, wherein a source connection is formed by forming then filling at least one via through the plurality of epitaxial layers to the conductive layer, a drain connection is formed by creating then filling at least one via through the plurality of epitaxial layers to the at least one drain contact, and a gate connection is formed by creating then filling at least one via through the plurality of epitaxial layers to the at least one gate contact.

9. The method as claimed in claim **1**, wherein patterned plating is performed before the at least one heat sink layer is formed.

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